REMARKS

Applicants respectfully request reconsideration of this application. Claims 1-28 were pending. Claims 1, 4-8, 12, 14, 17-18, 20-22, 24, 26, and 28 have been amended. Claims 3, 13, 19, and 25 have been canceled without prejudice. Claims 1-2, 4-12, 14-18, 20-24, and 26-28 remain pending.

The Office Action objected to the title for not being descriptive. Accordingly, Applicants have amended the title to be more descriptive. Withdrawal of the objection is respectfully requested.

The Office Action objected to the specification for minor informalities. Accordingly, Applicants have amended the specification to remove the informalities. Withdrawal of the objection is respectfully requested.

Claims 1, 12, and 24 have been rejected under 35 U.S.C. §102(e) as being anticipated by Verdun (U.S. Patent Application Publication No. 2005/0044448 A1). Applicants respectfully traverse the rejection.

Claim 1 as amended sets forth:

> ***de-asserting an indicator within a message packet*** to allow the processor to enter into the power state in response to a request from the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the chipset device exceeds a second threshold.

(Claim 1 as amended; emphasis added)

In contrast, Verdun fails to disclose at least the above limitation. According to Verdun, if memory controller hub determines that write tracking buffer is full, processor exits the non-snoopable lower power state (Verdun, paragraph [0019]). Verdun does not disclose de-asserting an indicator within a message packet to allow processor to enter into

the power state. Therefore, Verdun does not anticipate claim 1 as amended. Withdrawal

of the rejection is respectfully requested.

For the reason discussed above with respect to claim 1, Verdun does not anticipate

claims 12 and 24. Withdrawal of the rejection is respectfully requested.

Claims 1-17 and 24-28 have been rejected under 35 U.S.C. §102(e) as being

anticipated by Yavatkar et al. (U.S. Patent Application Publication No.

2003/0137945A1). Claims 3, 13, and 25 have been canceled without prejudice, thus

obviating the rejection. Applicants respectfully traverse the rejection on claims 1-2, 4-12,

14-17, 24, and 26-28.

Claim 1 as amended sets forth:

> ***de-asserting an indicator within a message packet*** to allow the processor to enter
> into the power state in response to a request from the processor to enter into the
> power state if a plurality of incoherent transactions pending in the buffer of the
> chipset device exceeds a second threshold.

(Claim 1 as amended; emphasis added)

In contrast, Yavatkar fails to disclose at least the above limitation. Yavatkar

merely discloses processing the packets with the receiver protocol state machine and

sending acknowledgments to the transmitter protocol state machine (Yavatkar, paragraph

[0018]). Yavatkar does not disclose, suggest, or imply de-asserting an indicator within a

message packet to allow the processor to enter into the power state. Therefore, Yavatkar

fails to anticipate claim 1 as amended.

Furthermore, Yavatkar fails to anticipate claim 1 as amended for the following

reason as well. Claim 1 sets forth that a processor exits a power state when a plurality of

coherent transactions pending in a buffer exceeds a *first threshold* and ***the processor***

enters into the power state if a plurality of ***incoherent*** transactions pending in ***the buffer***

exceeds a *second threshold*. In contrast, Yavatkar does not disclose the above limitation.
Yavatkar discloses *a transmitter protocol state machine 110* to wake up from a low
power state when an incoming packet buffer reaches a low water mark and *a receiver
protocol state machine 120* to switch into a high power mode when a buffer reaches a
high water mark (Yavatkar, paragraph [0018]). Note that the transmitter protocol state
machine 110 and the receiver protocol state machine 120 are distinct and separate from
each other (Yavatkar, Figure 1). However, claim 1 as amended sets forth *a processor* that
exits or enters a power state based on pending coherent or incoherent transactions in a
buffer exceeding a first or a second threshold, respectively. Moreover, claim 1
specifically recites "coherent transactions" and "incoherent transactions," whereas
Yavatkar makes no mention of coherent transactions and/or incoherent transactions.
Therefore, Yavatkar fails to disclose every limitation set forth in claim 1 as amended. For
at least these reasons, Yavatkar does not anticipate claim 1 as amended. Withdrawal of
the rejection is respectfully requested.

For the reason discussed above with respect to claim 1, Yavatkar does not
anticipate claims 12 and 24. Withdrawal of the rejection is respectfully requested.

Claims 2, 4-11, 14-17, and 26-28 depend, directly or indirectly, from claims 1, 12,
and 24, respectively. Thus, claims 2, 4-11, 14-17, and 26-28 are not anticipated by
Yavatkar for the reason discussed above with respect to claim 1. Withdrawal of the
rejection is respectfully requested.

Claims 18-23 have been rejected under 35 U.S.C. §103(a) as being unpatentable
over Wilcox (U.S. Patent Number 6,820,169) in view of Yavatkar. Claim 19 has been
canceled without prejudice, thus obviating the rejection. Applicants respectfully traverse
the rejection on claims 18 and 20-23.

Claim 18 as amended sets forth:

an input/output controller residing on a common substrate with the memory controller to allow a **processor** in the computing system to enter into the power state in response to a request from the processor to enter into a power state if a plurality of **incoherent transactions** pending in a buffer of the memory controller exceeds an entry threshold, to prevent the processor from entering into the power state if the plurality of **incoherent transactions** is below the entry threshold, and to cause the processor to exit from the power state if a plurality of **coherent transactions** pending in the buffer of the memory controller exceeds an exit threshold.

(Claim 18 as amended; emphasis added)

In contrast, neither Wilcox nor Yavatkar discloses the above limitation. As stated in the Office Action, Wilcox does not teach an input/output controller to allow a processor in the computing system to enter into the power state in response to a request from the processor to enter into a power state if a plurality of incoherent transactions pending in a buffer of the memory controller exceeds an entry threshold, to prevent the processor from entering into the power state if the plurality of incoherent transactions is below the entry threshold (Office Action, p. 10). Moreover, Yavatkar also fails to disclose the above limitation.

Yavatkar discloses *a transmitter protocol state machine 110* to wake up from a low power state when an incoming packet buffer reaches a low water mark and *a receiver protocol state machine 120* to switch into a high power mode when a buffer reaches a high water mark (Yavatkar, paragraph [0018]). Note that the transmitter protocol state machine 110 and the receiver protocol state machine 120 are distinct and separate from each other (Yavatkar, Figure 1). However, claim 1 as amended sets forth *a processor* that exits or enters a power state based on pending coherent or incoherent transactions in a

buffer exceeding a first or a second threshold, respectively. Moreover, claim 18 specifically recites "coherent transactions" and "incoherent transactions," whereas Yavatkar makes no mention of coherent transactions and/or incoherent transactions. Therefore, Yavatkar does not teach the above limitation of claim 18. Since neither Wilcox nor Yavatkar, alone or in combination, teaches the above limitation of claim 18, claim 18 as amended is patentable over Wilcox in view of Yavatkar. Withdrawal of the rejection is respectfully requested.

Claims 20-23 depend, directly or indirectly, from claim 18. Thus, claims 20-23 are patentable over Wilcox in view of Yavatkar for the reason discussed above with respect to claim 18. Withdrawal of the rejection is respectfully requested.

CONCLUSION

Applicants respectfully submit that the rejections have been overcome by the remarks, and that the pending claims are in condition for allowance. Accordingly, Applicants respectfully request the rejections be withdrawn and the pending claims be allowed.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: _____7/27_____, 2006

Chui-kiu Teresa Wong
Attorney for Applicants
Reg. No. 48,042

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300